WHAT IS CLAIMED IS:

1. A method for forming a hardmask comprising:

depositing at least one polymeric preceramic precursor film atop a substrate having at least one layer;

converting said at least one polymeric preceramic precursor film into at least one ceramic layer, said at least one ceramic layer having a composition of $Si_vN_wC_xO_yH_z$, where $0.1 \leq v \leq 0.9$, $0 \leq w \leq 0.5$, $0.05 \leq x \leq 0.9$, $0 \leq y \leq 0.5$, $0.05 \leq z \leq 0.8$ for $v+w+x+y+z=1$;

forming a patterned photoresist atop said at least one ceramic layer;

patterning said at least one ceramic layer to expose one or more regions of said underlying substrate, where a remaining region of said underlying substrate is protected by at least one patterned ceramic layer;

etching said one or more exposed region of said substrate.

2. The method of claim 1 wherein said substrate comprises at least one line level dielectric layer and at least one via level dielectric layer.

3. The method of claim 1 wherein said step a) of depositing said polymeric preceramic precursor film includes applying a solution of said polymeric preceramic precursor dissolved in an organic solvent, where said organic solvent is selected from the group consisting of: propylene glycol methyl ether acetate (PGMEA), propylene glycol methyl ether (PGME), toluene, xylenes, anisole, mesitylene, butyrolactone, cyclohexanone, hexanones, ethyl lactate, heptanones or combinations thereof.

4. The method of claim 3 wherein a solution comprising said preceramic precursor and solvent further comprises on or more selected from the group comprising: an adhesion promoter, a sacrificial moiety to produce porosity, an antistriation agent, or combinations thereof.

5. The method of claim 3 wherein said applying step is selected from the group consisting of: spin coating, spray coating, scan coating, and dip coating.

6. The method of claim 1 wherein said conversion of said polymeric preceramic precursor into said ceramic layer comprises thermal curing, electron irradiation, ion irradiation, irradiation with ultraviolet light, irradiation with visible light or combinations thereof.

7. The method of claim 1 further comprising the step of applying an adhesion promoter at either prior to application of said polymeric preceramic precursor, after application of said polymeric preceramic precursor, or after said conversion of said polymeric preceramic precursor into said ceramic layer.

8. The method of claim 1 wherein said at least one patterned ceramic layer comprises a hardmask, where said hardmask defines a via level dielectric and a line level dielectric in said substrate during said etching.

9. The method of claim 1 wherein said at least one patterned ceramic layer comprises a clustered hardmask, where said clustered hardmask comprises a bilayer having at least two distinct patterns and at least two distinct dielectric materials.

10. The method of claim 8 wherein a ceramic layer between said via level dielectric and said line level dielectric having a composition $Si_vN_wC_xO_yH_z$, where $0.05 \leq v \leq 0.8$, $0 \leq w \leq 0.9$, $0.05 \leq x \leq 0.8$, $0 \leq y \leq 0.8$, $0.05 \leq z \leq 0.8$ for $v+w+x+y+z=1$, is a buried etch stop.

11. The method of claim 1 wherein said at least one polymeric preceramic precursor film has a composition $Si_vN_wC_xO_yH_z$, where $0.1 \leq v \leq 0.8$, $0 \leq w \leq 0.8$, $0.05 \leq x \leq 0.8$, $0 \leq y \leq 0.3$, $0.05 \leq z \leq 0.8$ for $v+w+x+y+z=1$.

12. A multilayer interconnect structure for semiconducting devices comprising: at least one layer of patterned ceramic film having at least one composition $Si_vN_wC_xO_yH_z$, where $0.1 \leq v \leq 0.9$, $0 \leq w \leq 0.5$, $0.05 \leq x \leq 0.9$, $0 \leq y \leq 0.5$, $0.05 \leq z \leq 0.8$ for $v+w+x+y+z=1$, atop a substrate having one or more layers, where said one or more layers includes at least one metal layer.

13. The multilayer interconnect structure of claim 12, wherein said patterned ceramic film comprises at least two different silicon containing dielectrics having two distinct patterns, forming a clustered hardmask layer inlcuding a second hardmask layer atop a first hardmask layer.

14. The multilayer interconnect structure of claim 13, wherein said first hardmask layer defines a via level dielectric and said second hardmask layer defines a line level dielectric.

15. The multilayer interconnect structure of claim 12, wherein said substrate includes microelectronic interconnects and microelectronic devices.

16. The multilayer interconnect structure of claim 12, wherein said at least one patterned ceramic layer has a thickness from about 5 nm to about 300 nm.

17. The multilayer interconnect structure of claim 12, wherein the said at least one patterned ceramic layer contains porosity.

18. A multilayer interconnect structure comprising:

a multilayer substrate having at least a first dielectric layer and a second dielectric layer; where at least one ceramic buried etch stop having a composition $Si_vN_wC_xO_yH_z$, where $0.05 \leq v \leq 0.8$, $0 \leq w \leq 0.9$, $0.05 \leq x \leq 0.8$, $0 \leq y \leq 0.8$, $0.05 \leq z \leq 0.8$ for $v+w+x+y+z=1$, is between said first dielectric layer and said second dielectric layer.

19. The multilayer interconnect structure of claim 18, wherein the said first dielectric layer is a line level dielectric and said second dielectric layer is a via level dielectric.

20. The multilayer interconnect structure of claim 18 further comprising at least one patterned ceramic hardmask having composition $Si_vN_wC_xO_yH_z$, where $0.1 \leq v \leq 0.9$, $0 \leq w \leq 0.5$, $0.05 \leq x \leq 0.9$, $0 \leq y \leq 0.5$, $0.05 \leq z \leq 0.8$ for $v+w+x+y+z=1$, atop said substrate.